WHAT IS CLAIMED IS:

1. A memory device comprising at least one read control signal line for transmitting a read control signal to a memory cell, at least one read signal line for transmitting information of the memory cell to an outside according to activation of the read control signal corresponding to the read control signal line, at least one write control signal line for transmitting a write control signal to the memory cell, and at least one write signal line for transmitting external information to the memory cell according to activation of the write control signal corresponding to the write control signal line,

wherein the read signal line and the write signal line are alternately provided and the read control signal and the write control signal are controlled so as not to be activated at the same time.

2. The memory device according to claim 1, wherein the write control signal is activated after it is detected that the information of the memory cell is transmitted to the outside according to the activation of the read control signal.

3. The memory device according to claim 1, wherein the read control signal is deactivated after it is detected that the information of the memory cell is transmitted to the outside according to the activation of the read control signal.

4. The memory device according to claim 2 or 3, further comprising a dummy memory cell constituted by using a semiconductor element having the same shape as that of a semiconductor element forming the memory cell and having a circuit structure including a dummy read control signal line and a dummy read signal line having the same load characteristics as those of the read control signal line and the read signal

line respectively, the dummy memory cell outputting, to the dummy read signal line, a fixed storage value according to the activation of the read control signal given to the dummy read control signal line and the transmission of the information of the memory cell to the outside being detected by detection of the fixed storage value in the dummy read signal line.

5. The memory device according to claim 4, further comprising a dummy memory cell constituted by using a semiconductor element having the same shape as that of a semiconductor element forming the memory cell and having a circuit structure including a first dummy write control signal line having the same load characteristic as that of the write control signal line and serving to receive the read control signal, a second dummy write control signal line having the same load characteristic as that of the write control signal line and serving to receive the write control signal, a dummy write signal line having the same load characteristic as that of the write signal line and serving to receive a dummy write value, and a dummy write detection signal line having the same load characteristic as that of the read signal line, the dummy write value being written to the dummy memory cell corresponding to the activation of the read control signal, the dummy write value being inverted when it is detected that the dummy write value written to the dummy memory cell is output to the dummy write detection signal line, and the inverted dummy write value being written to the dummy memory cell according to the activation of the write control signal.

6. The memory device according to claim 5, wherein the write control signal is deactivated after it is detected that the dummy write value written to the dummy memory cell is output to the dummy write detection signal line.

7. The memory device according to claim 6, wherein the dummy

write value is given synchronously with a clock signal and the read control signal is then activated, thereby repeating a series of operations for writing the dummy write value to the dummy memory cell, reading a fixed storage value from the dummy memory cell, deactivating the read control signal, activating the write control signal, inverting the dummy write value by the detection of the output of the dummy write value written to the dummy memory cell, writing the inverted dummy write value to the dummy memory cell, and deactivating the write control signal.

8. The memory device according to claim 1, wherein the read control signal is activated after it is detected that the external information is transmitted to the memory cell according to the activation of the write control signal.

9. The memory device according to claim 1, wherein the write control signal is deactivated after it is detected that the external information is transmitted to the memory cell according to the activation of the write control signal.

10. The memory device according to claim 8 or 9, further comprising a dummy memory cell constituted by using a semiconductor element having the same shape as that of a semiconductor element forming the memory cell and having a circuit structure including a first dummy write control signal line, having the same load characteristic as that of the write control signal line and serving to receive the read control signal, a second dummy write control signal line having the same load characteristic as that of the write control signal line and serving to receive the write control signal, a dummy write signal line having the same load characteristic as that of the write signal line and serving to receive a dummy write value, and a dummy write detection signal line having the same load characteristic as that of the read signal line, the dummy write

value being written to the dummy memory cell according to the activation of the write control signal and the detection of the transmission of the external information to the memory cell depending on detection of output, to the dummy write detection signal line, of the dummy write value written to the dummy memory cell.

11. The memory device according to claim 10, wherein the dummy write value is inverted by the detection of the output, to the dummy write detection signal line, of the dummy write value written to the dummy memory cell, and the inverted dummy write value is written to the dummy memory cell according to the activation of the read control signal.

12. The memory device according to claim 10, further comprising a dummy memory cell constituted by using a semiconductor element having the same shape as that of a semiconductor element forming the memory cell and having a circuit structure including a dummy read control signal line and a dummy read signal line having the same load characteristics as those of the read control signal line and the read signal line respectively, the dummy memory cell outputting, to the dummy read signal line, a fixed storage value according to the activation of the read control signal given to the dummy read control signal line and the read control signal being deactivated by detection of the fixed storage value in the dummy read signal line.

13. The memory device according to claim 12, wherein the dummy write value is given synchronously with a clock signal and the write control signal is then activated, thereby repeating a series of operations for writing the dummy write value to the dummy memory cell, inverting the dummy write value by the detection of the written dummy write value in an output of the dummy memory cell, deactivating the write control signal, activating the read control signal, writing the inverted dummy write value to the

dummy memory cell, reading the fixed storage value from the dummy memory cell, and deactivating the read control signal.

14. The memory device according to claim 1, wherein the read control signal line and the write control signal line are provided as alternately as possible.

15. The memory device according to claim 1, wherein an absolute value of a substrate voltage of an MOSFET constituting a storage element in the memory cell is set to be greater than that of a signal voltage to be applied to the storage element at time of the activation of the read control signal.

16. The memory device according to claim 1, wherein an absolute value of a substrate voltage of a transfer gate in the memory cell is set to be greater than that of a signal voltage to be applied to a storage element at time of the activation of the read control signal.

17. The memory device according to claim 16, wherein a substrate voltage of a P-channel MOSFET of the transfer gate is raised.

18. The memory device according to claims 17, wherein a write control circuit for writing information to the memory cell in response to the write control signal includes an MOSFET which is constituted by a switch of the transfer gate having an inverting logic circuit to be controlled in response to the write control signal, and has a gate connected to an output of the inverting logic circuit, a drain connected to the write control signal line, and a source connected to a power supply or a ground.

19. The memory device according to claim 1, wherein a driving source of the write control signal line is provided with an MOSFET having a

gate connected to an input of an inverting logic gate for driving the read control signal line, a source connected to an output of a normal logic gate for inputting the write control signal, and a drain connected to the write control signal line.

20. The memory device according to claim 1, wherein an MOSFET having a gate connected to an output of an inverting logic gate for inputting the read control signal, a source connected to the output of the normal logic gate for inputting the write control signal and a drain connected to the write control signal line is provided in a middle section or an end of the write control signal line.

21. A memory device wherein a storage element in a memory cell is constituted by first and second inverting logic gates, a reset signal line is connected to a first source of the first inverting logic gate, a reset signal to be sent to the reset signal line is fixed to be inactive during a reading and writing operation of the memory cell, and the reset signal is activated to set a state of the storage element to have a desirable value for a period other than the reading and writing operation.

22. The memory device according to claim 21, wherein when a first source and a second source of the second inverting logic gate are to correspond to the first source and a second source of the first inverting logic gate, an inverting reset signal line for sending an inverted reset signal is connected to the second source of the second inverting logic gate.

23. The memory device according to claim 21, wherein the reset signal is activated in response to a signal indicative of completion of write to the memory cell.

24. A memory device wherein a storage element in a memory cell is

constituted by first and second inverting logic gates, a NOT signal of AND of a write control signal and a write signal is connected to a first source of a transistor constituting the first inverting logic gate, an AND signal of a write control signal and an inverted write signal is connected to a second source of the transistor constituting the first inverting logic gate, a NOT signal of AND of the write control signal and the inverted write signal is connected to a first source of a transistor constituting the second inverting logic gate, and an AND signal of the write control signal and the write signal is connected to a second source of the transistor constituting the second inverting logic gate.

25. The memory device according to claim 24, wherein there is provided a combination of the write control signals and the write signals, the storage element in the memory cell is constituted by using a combination of two inverting logic gates of which number is equal to the number of the write control signals and which are caused to correspond to the write control signals, gates and drains of the transistors constituting the respective inverting logic gates have corresponding points connected in parallel with each other, and the sources of the transistors constituting the respective inverting logic gates are connected to signals generated by the write control signal and the write signal which correspond to the respective inverting logic gates.